042390.P17811 Patent

ABSTRACT

[0048] An embodiment of the invention reduces the external resistance of a transistor by utilizing a silicon germanium alloy for the source and drain regions and a nickel silicon germanium self-aligned silicide (i.e., salicide) layer to form the contact surface of the source and drain regions. The interface of the silicon germanium and the nickel silicon germanium silicide has a lower specific contact resistivity based on a decreased metal-semiconductor work function between the silicon germanium and the silicide and the increased carrier mobility in silicon germanium versus silicon. The silicon germanium may be doped to further tune its electrical properties. A reduction of the external resistance of a transistor equates to increased transistor performance both in switching speed and power consumption.